GP/2826

Docket No. 740756-2138

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
Takayuki IKEDA et al.	)	Examiner: Ahmed N. SEFER
Serial No. 09/542,473	)	
Filed: April 4, 2000	)	Group Art Unit: 2826
For: ELECTROOPTICAL DEVICE AND A METHOD	)	Confirmation No. 6069
OF MANUFACTURING THE SAME	)	

#22 Letter FJONES 10-25-02

Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on September 25, 2002.

Bonnie L. Garilli

Name: Bonnie L. Garilli

SECOND REQUEST FOR ACKNOWLEDGMENT OF INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

An Information Disclosure Statement with Form PTO-1449 was filed in the above-identified patent application on September 4, 2001. Applicants have not yet received back from the Examiner a copy of the Form PTO-1449 initialed to acknowledge the fact that the Examiner has considered the cited disclosed information.

The Examiner is requested to initial and return to the undersigned a copy of the subject Form PTO-1449.

Should there be any questions concerning this communication, please telephone the undersigned at the number set forth below.

Respectfully submitted,

Jeffrey L. Costellia
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Form PTO-1449 (Rev. 8-83)	Department of Commerce Patent and Trademark Office	Atty Docket 0756-[redacted]	Serial No. 09/542,473
INFORMATION DISCLOSURE STATEMENT		Applicants: Takayuki IKEDA	
		Filing Date: April 04, 2000	Group Art Unit: 2826

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date (if appropriate)
	6,013,929	01/11/2000	Ohtani			

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner Initial	
	Specifications and Drawings for Application Serial No. 08/862,895, "Semiconductor Intergrated Circuit and Fabrication Method Thereof", Filing Date: May 23, 1997, Inventor: Hisashi OHTANI
	Specifications and Drawings for Application Serial No. 09/468,859, "Thin Film Transistor, Method of Manufacturing the Same, and Semiconductor Device Including the Same" Filing Date: December 21, 1999, Inventor: Hisashi OHTANI
	Specifications and Drawings for Application Serial No. 09/487,432, "Semiconductor Device and Process for Production Thereof" Filing Date: January 19, 2000, Inventors: Shunpei YAMAZAKI et al.
	Specifications and Drawings for Application Serial No. 09/493,411, "Semiconductor Device and Method of Fabricating the Same" Filing Date: January 28, 2000, Inventors: Shunpei YAMAZAKI et al.

Examiner	Date Considered

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.